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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/960,560	09/21/2001	Samuel W. Sheng	01-319 / 1496.00134	5708
24319	7590	11/17/2005	EXAMINER	
LSI LOGIC CORPORATION 1621 BARBER LANE MS: D-106 MILPITAS, CA 95035			ENG, GEORGE	
			ART UNIT	PAPER NUMBER
			2688	

DATE MAILED: 11/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/960,560

Applicant(s)

SHENG ET AL.

Examiner

George Eng

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 August 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

1. This Office action is in response to the amendment filed 8/5/2005.

Drawings

2. The drawings were received on 8/5/2005. These drawings are acceptable.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-7 and 9-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cranford, Jr. et al. (US PAT. 5,940,441 hereinafter Cranford) in view of Phanse (US PAT. 6,823,028).

Regarding claim 1, Cranford discloses an apparatus (100, figure 1) for equalizing a communication signal (112, figure 1), i.e., an analog input, transmitted through a transmission medium (110, figure 1) comprising a first circuit (102, figure 1) for filtering the communication signal in an analog domain in response to one or more control signals (116, figure 1), a second circuit (202, figure 2) for converting the communication signal to a first digital signal, and a third circuit (204, figure 2) configured to generate one or more control signals (210 and 212 figure 2) in response to the first digital signal, wherein the third circuit is configured to adjust (i.e., deliberately skew) the transfer characteristics (i.e., the filter tuning of the analog input signal) within the first circuit thereby compensating for loss and distortion of the signal caused by the transmission medium (abstract and col. 3 line 34 through col. 5 line 15). Cranford differs from the claimed invention in not specifically teaching the third circuit configured to generate a second digital signal and to deliberately skew the analog input signal within the first circuit in response to a signal to-noise ratio of the first digital signal to partially compensate for frequency dependent effects. However, Phanse teaches an apparatus for use in an analog front end of a receiver comprising a circuit (175 and 180, figure 1) to generate a second signal (i.e., signal to digital FIR filter 175, figure 1), and to deliberately skew the analog input signal within a first circuit (140, figure 1) in response to a signal-to-noise ratio (generated from a slicer 155, figure 1) of a first digital signal (obtained from ADC 145, figure 1) to partially compensate for frequency

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dependent effects, thereby improving the performance of full-duplex transceiver front ends to compensate for operational changes due to frequency effects associated with a transmission medium (col. 3 lines 29-44, col. 6 lines 20-39 and col. 9 line 53 through col. 10 line 60). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Cranford in having the third circuit configured to generate a second digital signal and to deliberately skew the analog input signal within the first circuit to control filter tuning to partially compensate for frequency dependent effects, as per teaching of Bickley, because it improves the apparatus by providing precise tuning of very narrow bandwidth filters.

Regarding claims 2-4, Cranford discloses the third circuit including a first processor (204, figure 2) configured to generate one or more control signals and to provide back-end digital processing control over the first circuit, wherein the first circuit is configured to provide partial adaptation of the communication signal in the analog domain (col. 2 lines 18-30 and col. 3 lines 57-62).

Regarding claim 5, Phanse teaches the AEF (140, figure 1), read as the first circuit comprising a filter configured to tune the analog input signal and a processor (175, figure 1) configured to calibrate the filter to provide signal equalization (col. 6 lines 13-15) so that one skill in the art would recognize the processor being configured to calibrate the filter to a center frequency prior to the deliberate skewing.

Regarding claim 6, Phanse teaches the third circuit (175 and 180, figure 1) being configured to offset the center frequency of the filter of the first circuit (col. 4 lines 23-58).

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Regarding claim 7, Cranford discloses the first circuit comprising an analog filter (102, figure 1), the second circuit comprising an analog-to-digital conversion circuit (202, figure 2), and Phase teaches the third circuit comprising an equalizer circuit (150, figure 1) and a digital signal processing device (180, figure 1) to generate the control signals and adapted a tuning code of the equalizer circuit.

Regarding claim 9, the limitations of the claim are rejected as the same reasons set forth in claim 1.

Regarding claim 10, the limitations of the claim are rejected as the same reasons set forth in claim 1.

Regarding claim 11, the limitations of the claim are rejected as the same reasons set forth in claims 2-4.

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Regarding claims 12-13, the limitations of the claim are rejected as the same reasons set forth in claims 5-6.

Regarding claim 14, Phanse teaches to generate the second digital signal with an adaptive filter-impulse response filter equalizer (col. 5 lines 36-38 and col. 6 lines 22-24).

Regarding claim 15, Cranford teaches to generate the control signals (V_G , V_C , figure 2) with digital signal processing device (204, figure 2).

Regarding claim 16, Phanse teaches adapting a tuning code of the filter and the filtering and said FIR equalizer with digital processing device to optimize a channel response (col. 10 lines 25-38).

Regarding claim 17, Phanse teaches to partially adapting the tuning code of the filter device in the analog domain (col. 9 line 53 through col. 10 line 4).

Regarding claim 18, the limitations of the claim are rejected as the same reasons set forth in claim 14.

Regarding claims 19-20, Phanse teaches to reduce the dynamic range needed in the analog-to-digital converter circuit by the deliberate skewing of the analog input signal, wherein the deliberate skewing reduces the number of taps needed in the FIR equalizer circuit (col. 10 lines 5-67).

5. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cranford, Jr. et al. (US PAT. 5,940,441 hereinafter Cranford) in view of Phanse (US PAT. 6,823,028) as applied in claim 1 above, and further in view of English (US PAT. 5,489,879).

Regarding claim 8, Cranford discloses the filter (102, figure 4) comprising a current source, a digital switched capacitor array circuit (C, figure 4), a rectifier (G, figure 4) and an analog-to-digital converter (208, figure 2) to compensate for semiconductor process variations (col. 4 lines 9-27 and col. 7 line 1 through col. 10 line 61). Although the combination of Cranford and Phanse does not specifically disclose the digitally switched capacitor array circuit, the rectifier and the analog-to-digital converter being configured to sweep over code values and determine a center value, it is old and notoriously well known in the art of operating a filter components including the digitally switched capacitor array circuit, the rectifier and the analog-to-digital converter to compensate for frequency-dependent characteristics and provide a high quality subcarrier signal by sweeping over code values and determine a center value, thereby the subcarrier signal produced more closely matches the desire shape and center frequency, for example see English (col. 3 line 42 through col. 5 line 21). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Cranford and Phanse in having the digitally switched capacitor array circuit, the rectifier and the analog-to-digital converter being configured to sweep over code values and determine a center value, as per teaching of English, because it compensates for frequency-dependent characteristics and provides a high quality subcarrier signal so that the subcarrier signal produced more closely matches the desire shape and center frequency.

Response to Arguments

6. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to George Eng whose telephone number is (571) 272-7495. The examiner can normally be reached on Tue-Fri 7:30 AM-6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Curtis A. Kuntz can be reached on (571) 272-7499. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



George Eng
Primary Examiner
Art Unit 2643